Customer No.: 31561
Docket No.:13154-US-PA
Application No.: 10/710,931

REMARKS

Present Status of the Application

The Office Action rejected present pending claims 1-11. Specifically, the Office Action rejected claims 6-11 under 35 U.S.C. 112, second paragraph. The Office Action rejected claims 1, 3-6, and 8-11 under 35 U.S.C. 102(b) as being anticipated by Yamagata (U. S. Patent 5,158,899). The Office Action rejected claims 1-3, 5-8, 10 and 11 under 35 U.S.C. 102(b) as being anticipated by Steinhoff et al. (U. S. Patent 6,424,013; hereinafter Steinhoff). The Office Action also objects claims 1 and 6. Applicant amended claims to overcome objections and rejections under 35 U.S.C. 112, second paragraph without change the scope or giving up the possibility under doctrine of equivalent. Applicant has also added claims 12-13. After entry of the foregoing amendments, claims 1-13 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Claim Rejections under 35 USC 112

Applicant has amended claims to correct typo errors and improve clarity. Amendments are not subjected to reducing scope and estoppel.

Discussion of Claim Rejections under 35 USC 102

The Office Action rejected claims 1, 3-6, and 8-11 under 35 U.S.C. 102(b) as being anticipated by Yamagata. The Office Action rejected claims 1-3, 5-8, 10 and 11 under 35 U.S.C. 102(b) as being anticipated by Steinhoff. Applicant respectively traverses the rejections for at

least the reason set for the below.

1. In the present invention, independent claims 1 and 6, as for example shown in FIG. 2 and FIG. 3, has recited the features to create the first BJT 216 (316, 318) and the second BJT 218 (320), under the circuit connection. The drain region, as recited in claims 1 and 6, is a common drain for the two parasitic BJT's.

In addition, when the ESD current enters from the drain, the ESD current is channeled to the common voltage, which for example, is a ground voltage. In other words, under the structure of the claimed invention, the ESD current can be channeled by two parasitic BJT's in protection mechanism.

2. In re Yamagata (Fig. 1E), has shown the structure with ***only one BJT 11 being created.*** Therefore, Yamagata does not disclose the structure of the present invention to create two parasitic BJT's.

Furthermore, with respect to claims 12-13 with defining the common voltage as the ground voltage, when the ESD current enters the BJT 11 from the drain region 8, the current is channeled to the system voltage Vcc (doped region 10). The system voltage Vcc is the high voltage Vcc and is not the common voltage of the present invention, such as the ground voltage.

In other words, the claimed MOS ESD device in the present invention is always off except when the ESD occurs and create the parasitic BJT's. In Yamagata, the collector terminal of the BJT 11 is coupled to the VCC while the base terminal of the BJT 11 is applied the negative voltage VBB (col. 6, line 50). In other words, the circuit created by Yamagata is different from

the present invention.

For at least the foregoing reasons, independent claims 1 and 6 have patently defined over the prior art and should be allowed. For at least the same reasons, dependent claims 2-5 and 7-13 patently define over the prior art reference as well.

3. In re Steinhoff, Fig. 3B has disclosed only one BJT, which is composed by doped regions 350 and 352 with the substrate 338. Under the connection of Steinhoff, the circuit is shown in FIG. 5, in which the drain of the BJT 510 (350+352+338) is coupled to the bond pad 300. Clearly, *only one BJT is disclosed in Steinhoff.* ***Steinhoff does not disclose the second BJT of the present invention.***

The Office Action states that the drains region 352, the substrate 338 and the N-type layer 340 can form the second BJT of the present invention. However, Applicant respectfully disagrees.

In FIG. 3B and FIG. 5, clearly, the substrate 338 and the N-type layer 340 are used to create the parasitic capacitor Cpn (326, 314) and the parasitic diode D1 (324, 312). In other words, Steinhoff indeed failed to disclose the second BJT, as recited in claims 1 and 6.

Applicant also respectfully reminds that hindsight should not be involved in considering the patentability.

For at least the foregoing reasons, independent claims 1 and 6 have patently defined over the prior art and should be allowed. For at least the same reasons, dependent claims 2-5

and 7-13 patently define over the prior art reference as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-13 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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